



# Dual Matched High Performance Operational Amplifiers

## OP-04/OP-14

### FEATURES

- Excellent DC Input Specifications
- Matched  $V_{OS}$  and CMRR
- OP-14 Fits Standard 1458/1558 Sockets
- Internally Compensated
- Low Noise
- Low Drift
- Low Cost
- $0^{\circ}\text{C}/+70^{\circ}\text{C}$  and  $-55^{\circ}\text{C}/+125^{\circ}\text{C}$  Models
- Silicon-Nitride Passivation
- Models with MIL-STD-883 Class B Processing Available From Stock
- Available in Die Form

### ORDERING INFORMATION †

$T_a = +25^{\circ}\text{C}$ $V_{OS}$ MAX (mV)	PACKAGE					OPERATING TEMPERATURE RANGE
	TO-99	TO-100	8-PIN	14-PIN	8-PIN	
0.75	OP14AJ*	OP04AK*	OP14AZ*	OP14AY*	—	MIL
0.75	OP14EJ	—	OP14EZ	OP04EY	OP14EP	COM
2.0	OP14J	OP04K*	OP14Z*	OP04AY	—	MIL
2.0	OP14CJ	OP04CK	OP14CZ	OP04CY	OP14CP	XIND
2.0	—	—	—	—	OP14CS	XIND
5.0	—	OP04BK	—	—	—	MIL
5.0	OP14DJ	—	—	—	OP14DP	XIND

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

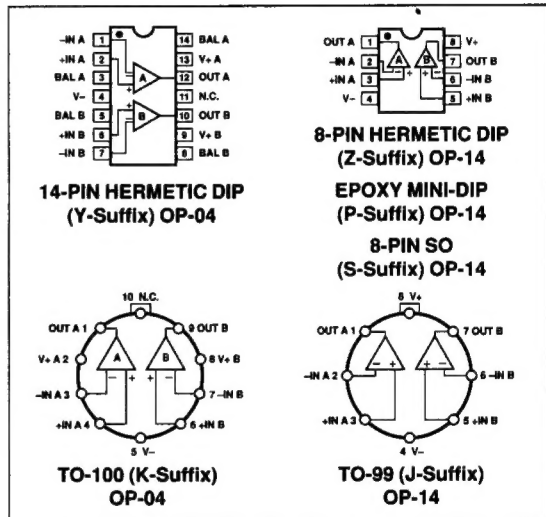
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

### GENERAL DESCRIPTION

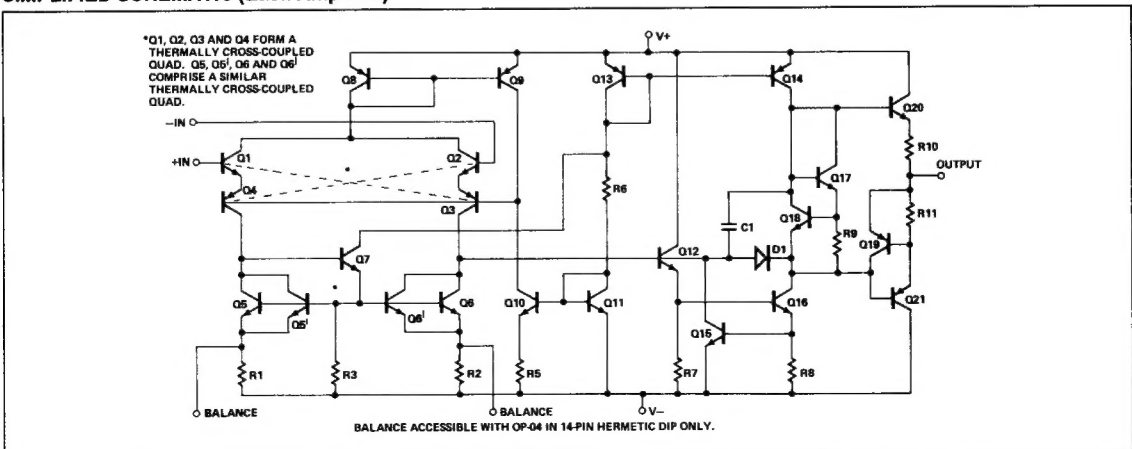
The OP-04/OP-14 series of dual general-purpose operational amplifiers provides significant improvements over industry-standard 747 and 1458/1558 (OP-14) types while maintaining

pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as  $V_{OS}$ ,  $I_{OS}$ ,  $I_B$ , CMRR, PSRR and  $A_{VO}$ , are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise". A thermally-symmetrical input stage design provides low  $TCV_{OS}$ ,  $TCI_{OS}$ , and insensitivity to output load conditions. This series is ideal for upgrading existing designs where accuracy improvements are desired. For more stringent requirements, refer to the OP-200, OP-207, OP-220, or OP-221 dual-matched operational amplifier data sheets.

### PIN CONNECTIONS



### SIMPLIFIED SCHEMATIC (Each Amplifier)



## OP-04/OP-14

### ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .....	±22V
Differential Input Voltage .....	±30V
Input Voltage .....	Supply Voltage
Output Short-Circuit Duration .....	Indefinite
Storage Temperature Range	
J, K, Y, and Z Packages .....	–65°C to +150°C
P Package .....	–65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) .....	300°C
Operating Temperature Range	
A, Plain, B-Suffix .....	–55°C to +125°C
E-Suffix .....	0°C to +70°C
C, D-Suffix .....	–40°C to +85°C
Junction Temperature ( $T_J$ ) .....	–65°C to +150°C

PACKAGE TYPE	$\theta_{JA}$ (Note 2)	$\theta_{JC}$	UNITS
TO-99 (J)	150	18	°C/W
TO-100 (K)	142	21	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
14-Pin Hermetic DIP (Y)	108	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

#### NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2.  $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for TO, CerDIP, and P-DIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

### MATCHING CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A OP-04E OP-14A OP-14E			OP-04 OP-04C OP-14 OP-14C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	$\Delta V_{OS}$	$R_S \leq 20k\Omega$	—	0.3	1	—	1	2	mV
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$ , $R_S \leq 100\Omega$	94	106	—	94	106	—	dB

### MATCHING CHARACTERISTICS at $V_S = \pm 15V$ , $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-04A, OP-14A, OP-04 and OP-14, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-04E, OP-14E, $-40^\circ C \leq T_A \leq +85^\circ C$ for OP-04C and OP-14C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A OP-04E OP-14A OP-14E			OP-04 OP-04C OP-14 OP-14C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	$\Delta V_{OS}$	$R_S \leq 20k\Omega$	—	0.5	1.5	—	1.5	3	mV
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$ , $R_S \leq 100\Omega$	90	100	—	90	100	—	dB

### ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	$I_{OS}$		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	$I_B$		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	$R_{IN}$	(Note 3)	2.0	7.5	—	1.35	7	—	1	5	—	M $\Omega$
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

**ELECTRICAL CHARACTERISTICS (Each Amplifier) at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted. (Continued)**

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	200	—	V/mV
Power Consumption (Note 2)	$P_d$	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	$e_{np-p}$	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	$\mu V_{p-p}$
Input Noise Voltage Density	$e_n$	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	$i_{np-p}$	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	$pA_{p-p}$
Input Noise Current Density	$i_n$	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$ , $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ $\mu s$
Large-Signal Bandwidth (Notes 1, 5)		$V_O = 20V_{p-p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1.0$	1.0	1.3	—	1.0	1.3	—	1.0	1.3	—	MHz
Risetime (Note 1)	$t_r$	$A_V = +1$ , $V_{IN} = 50mV_{p-p}$ $R_L = 2k\Omega$ , $C_L = 50pF$	—	260	350	—	260	350	—	260	350	ns
Overshoot (Note 1)	OS	$A_V = +1$ , $V_{IN} = 50mV_{p-p}$ $R_L = 2k\Omega$ , $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

**ELECTRICAL CHARACTERISTICS (Each Amplifier) at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$ , unless otherwise noted.**

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	$TCV_{OS}$	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	$I_{OS}$		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	$TCI_{OS}$		—	7.5	120	—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	$I_B$		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		$\pm 10$	$\pm 13$	—	$\pm 10$	$\pm 13$	—	$\pm 10$	$\pm 13$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	$\pm 10$	$\pm 13$	—	V

**NOTES:**

1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by input bias current.
4. Guaranteed by maximum risetime.
5. Guaranteed by minimum slew rate.

# OP-04/OP-14

**ELECTRICAL CHARACTERISTICS (Each Amplifier)** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04E/OP-14E			OP-04C/OP-14C			OP-14D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	$I_{OS}$		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	$I_B$		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	$R_{IN}$	(Note 3)	2.0	7.5	—	1.35	7	—	1	5	—	M $\Omega$
Input Voltage Range	IVR		$\pm 10$	$\pm 13$	—	$\pm 10$	$\pm 13$	—	$\pm 10$	$\pm 13$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	V
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption (Note 2)	$P_d$	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	$e_{np-p}$	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	$\mu V_{p-p}$
Input Noise Voltage Density	$e_n$	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	$i_{np-p}$	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	$pA_{p-p}$
Input Noise Current Density	$i_n$	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$ , $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ $\mu s$
Large-Signal Bandwidth (Notes 1, 5)		$V_O = 20V_{p-p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1$	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime (Note 1)	$t_r$	$A_V = +1$ , $V_{IN} = 50mV$ $R_L = 2k\Omega$ , $C_L = 50pF$	—	260	350	—	260	350	—	260	350	ns
Overshoot (Note 1)	OS	$A_V = +1$ , $V_{IN} = 50mV$ $R_L = 2k\Omega$ , $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

## NOTES:

1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by input bias current.
4. Guaranteed by maximum risetime.
5. Guaranteed by minimum slew rate.

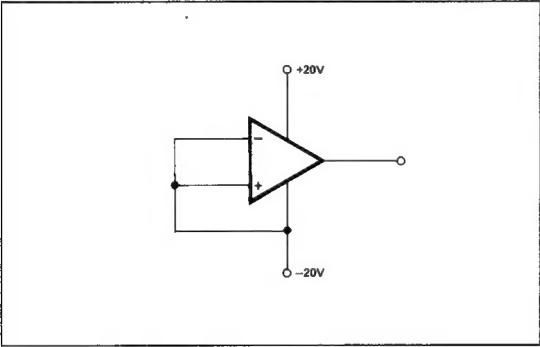
**ELECTRICAL CHARACTERISTICS (Each Amplifier)** at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$  for E,  $-40^\circ C$  to  $+85^\circ$  for C and D, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04E/OP-14E			OP-04C/OP-14C			OP-14D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	$TCV_{OS}$	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	$I_{OS}$		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	$TCI_{OS}$		—	7.5	120	—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	$I_B$		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		$\pm 10$	$\pm 13$	—	$\pm 10$	$\pm 13$	—	$\pm 10$	$\pm 13$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12$	$\pm 13$	—	$\pm 12$	$\pm 13$	—	$\pm 10$	$\pm 13$	—	V

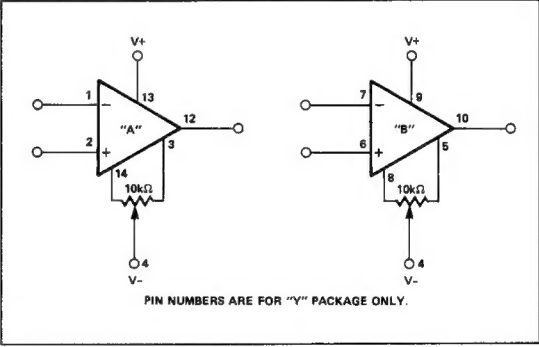
**NOTES:**

1. Sample tested.

**BURN-IN CIRCUIT (1/2 of OP-04, OP-14)**

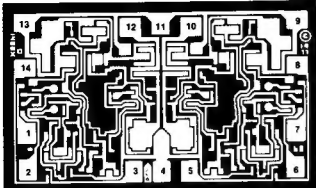


**OFFSET ADJUST CIRCUIT**



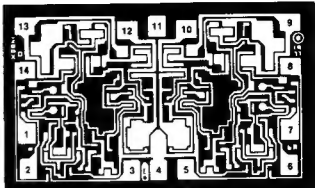
# OP-04/OP-14

## DICE CHARACTERISTICS



**OP-14**

**DIE SIZE 0.080 × 0.050 inch, 4000 sq. mils**  
(2.03 × 1.27 mm, 2.58 sq. mm)



**OP-04**

1. INVERTING INPUT (A)  
2. NONINVERTING INPUT (A)  
3. BALANCE (A)  
4. V-  
5. BALANCE (B)  
6. NONINVERTING INPUT (B)  
7. INVERTING INPUT (B)

8. BALANCE (B)  
9. V+  
10. OUTPUT (B)  
11. V+  
12. OUTPUT (A)  
13. V+  
14. BALANCE (A)

1. INVERTING INPUT (A)  
2. NONINVERTING INPUT (A)  
3. BALANCE (A)  
4. V-  
5. BALANCE (B)  
6. NONINVERTING INPUT (B)  
7. INVERTING INPUT (B)

8. BALANCE (B)  
9. V+ (B)  
10. OUTPUT (B)  
11. NO CONNECTIONS  
12. OUTPUT (A)  
13. V+ (A)  
14. BALANCE (A)

**NOTE:** 9, 11 and 13 are internally connected.

**WAFER TEST LIMITS** at  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N LIMIT	OP-04G OP-14G LIMIT	UNITS
Input Offset Voltage	$V_{OS}$	$R_S \leq 20k\Omega$	0.75	2	mV MAX
Input Offset Voltage Match	$\Delta V_{OS}$	$R_S \leq 20k\Omega$	1	2	mV MAX
Input Offset Current	$I_{OS}$		5	5	nA MAX
Input Bias Current	$I_B$		50	75	nA MAX
Input Voltage Range	IVR		$\pm 10$	$\pm 10$	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	80	dB MIN
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$ $R_S \leq 100\Omega$	94	94	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	100	$\mu V/V$ MAX
Output Voltage Swing	$V_O$	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	$\pm 12$ $\pm 12$	$\pm 12$ $\pm 12$	V MIN
Large-Scale Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	50	V/mV MIN
Power Consumption (Both Amplifiers)	$P_d$	$V_O = 0$	170	170	mW MAX
Channel Separation	CS		100	100	dB MIN

### NOTE:

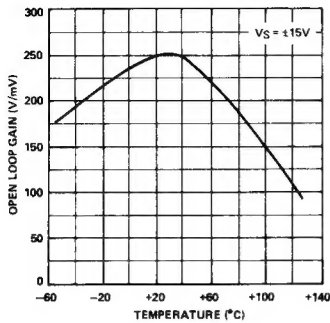
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

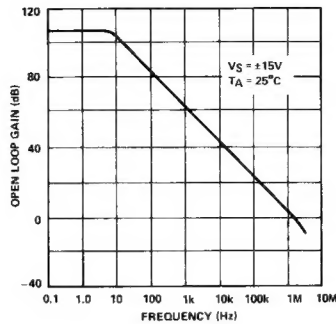
PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N LIMIT	OP-04G OP-14G LIMIT	UNITS
Risetime	$t_r$	$A_V = +1$ , $V_{IN} = 50mV$ , $R_L = 2k\Omega$ , $C_L = 50pF$	200	200	ns
Overshoot	OS	$A_V = +1$ , $V_{IN} = 50mV$ , $R_L = 2k\Omega$ , $C_L = 50pF$	5	5	%
Slew Rate	SR	$R_L = 2k\Omega$ , $C_L = 100pF$	0.25	0.25	V/ $\mu s$

TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

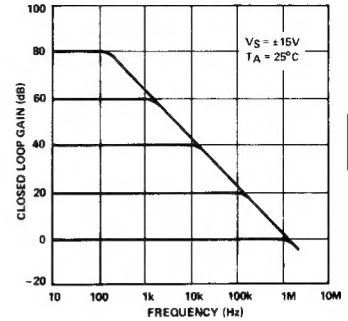
OPEN-LOOP GAIN  
vs TEMPERATURE



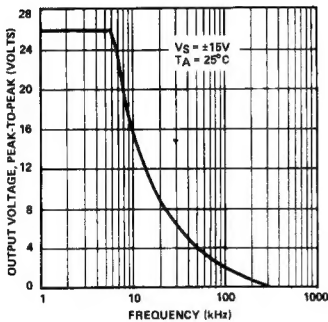
OPEN-LOOP  
FREQUENCY RESPONSE



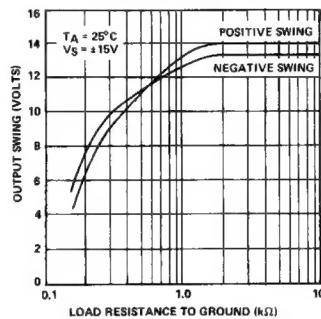
CLOSED-LOOP RESPONSE  
FOR VARIOUS  
GAIN CONFIGURATIONS



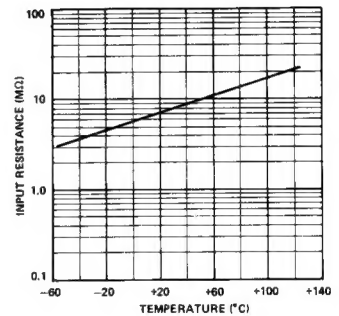
MAXIMUM UNDISTORTED  
OUTPUT vs FREQUENCY



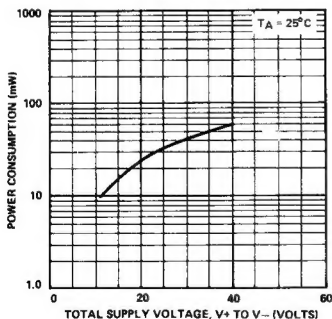
OUTPUT VOLTAGE vs  
LOAD RESISTANCE



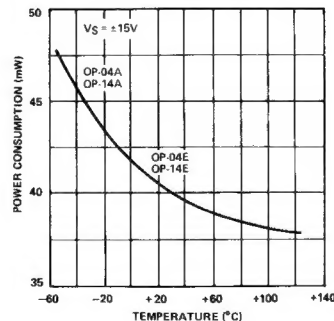
INPUT RESISTANCE  
vs TEMPERATURE



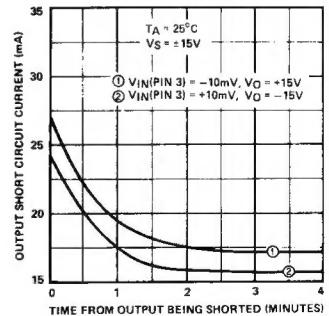
POWER CONSUMPTION  
vs POWER SUPPLY



POWER CONSUMPTION  
vs TEMPERATURE



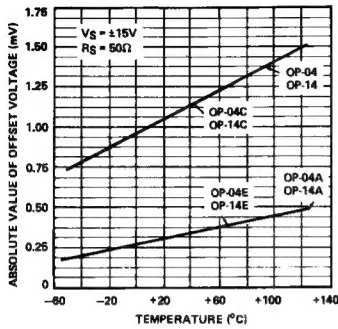
OUTPUT SHORT-CIRCUIT  
CURRENT vs TIME



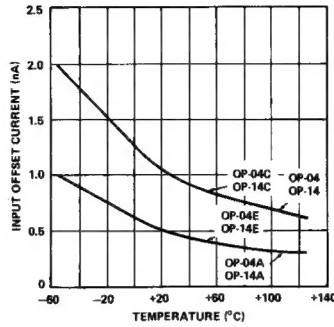
# OP-04/OP-14

## TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

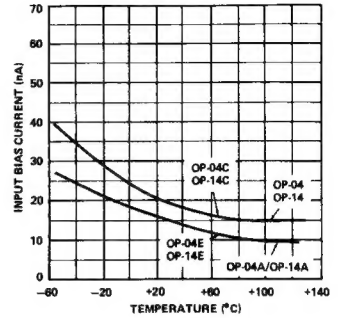
**UNTRIMMED OFFSET VOLTAGE  
vs TEMPERATURE**



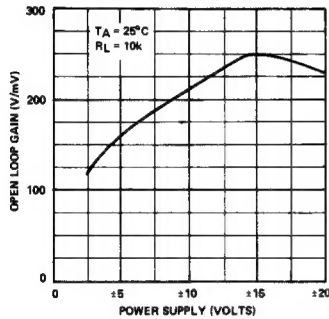
**INPUT OFFSET CURRENT  
vs TEMPERATURE**



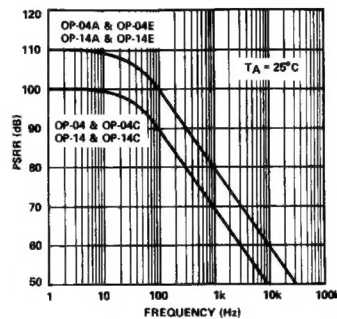
**INPUT BIAS CURRENT  
vs TEMPERATURE**



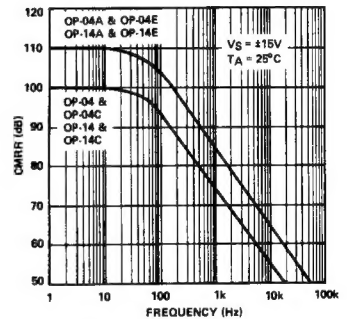
**OPEN-LOOP GAIN vs  
POWER SUPPLY VOLTAGE**



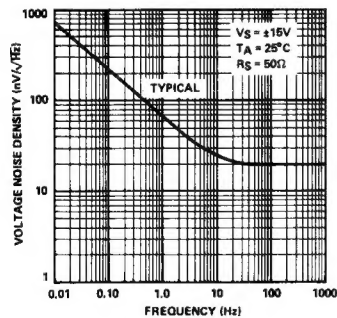
**PSRR vs FREQUENCY**



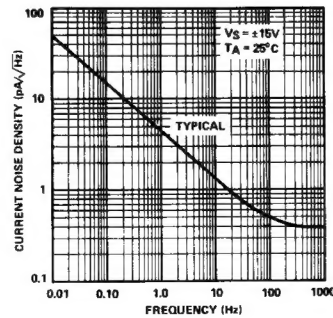
**CMRR vs FREQUENCY**



**INPUT SPOT NOISE  
VOLTAGE vs FREQUENCY**



**INPUT SPOT NOISE  
CURRENT vs FREQUENCY**



**INPUT WIDEBAND NOISE vs  
BANDWIDTH (0.1Hz TO  
FREQUENCY INDICATED)**

